WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a semiconductor substrate;

a memory cell capacitor for storing data, including a first electrode provided above the semiconductor substrate, a capacitance insulating film formed on the first electrode, and a second electrode provided on the capacitance insulating film;

a step reducing film covering an upper surface and a side surface of the memory cell capacitor; and

an overlying hydrogen barrier film covering the step reducing film.

2. The semiconductor memory device of claim 1, wherein the step reducing film is formed by an atmospheric pressure thermal CVD method using O_3 and TEOS.

3. The semiconductor memory device of claim 1, wherein the overlying hydrogen barrier film is formed by a sputtering method.

4. The semiconductor memory device of claim 1, further comprising an underlying hydrogen barrier film provided under the first electrode.

5. The semiconductor memory device of claim 4, wherein the underlying hydrogen barrier film is in contact with the overlying hydrogen barrier film in a peripheral region around the memory cell capacitor.

6. The semiconductor memory device of claim 5,

wherein the overlying hydrogen barrier film and the underlying hydrogen barrier film are patterned so as to have substantially the same outer shape.

7. The semiconductor memory device of claim 5, wherein the overlying hydrogen barrier film includes a barrier film covering an upper surface of the step reducing film and a side wall covering a side surface of the step reducing film.

8. The semiconductor memory device of claim 4, wherein the first electrode is buried in the underlying hydrogen barrier film.

9. The semiconductor memory device of claim 8, wherein the first electrode includes a conductive hydrogen barrier film in a lower portion thereof.

10. A method for manufacturing a semiconductor memory device, comprising the steps of:

(a) forming a memory cell capacitor above a semiconductor substrate, the memory cell capacitor including a first electrode, a capacitance insulating film formed on the first electrode, and a second electrode provided on the capacitance insulating film;

(b) after the step (a), forming a step reducing film on the substrate so as to cover the memory cell capacitor; and

(c) forming an overlying hydrogen barrier film on the substrate so as to cover the step reducing film.

11. The method for manufacturing a semiconductor memory device of claim 10, further comprising the step of:

(d) before the step (a), forming an underlying hydrogen barrier film above the semiconductor substrate,

wherein in the step (a), the first electrode is formed on the underlying hydrogen barrier film.

12. The method for manufacturing a semiconductor memory device of claim 11, further comprising the step of:

(e) after the step (b), removing the step reducing film in a peripheral region around the memory cell capacitor,

wherein in the step (c), the overlying hydrogen barrier film is formed so as to be in contact with the underlying hydrogen barrier film in the peripheral region around the memory cell capacitor.

13. The method for manufacturing a semiconductor memory device of claim 12, wherein a wet etching method is employed in the step (e).

14. The method for manufacturing a semiconductor memory device of claim 12, further comprising the step of:

(f) after the step (e), patterning the overlying hydrogen barrier film and the underlying hydrogen barrier film in the peripheral region around the memory cell capacitor by using the same mask.

15. The method for manufacturing a semiconductor memory device of claim 11, further comprising the steps of:

(g) after the step (c), removing the step reducing

film and the overlying hydrogen barrier film in the peripheral region around the memory cell capacitor so as to expose the underlying hydrogen barrier film;

(h) forming a second overlying hydrogen barrier film on the substrate; and

(i) etching back the second overlying hydrogen barrier film so as to form a side wall covering a side surface of the overlying hydrogen barrier film and a side surface of the step reducing film.

16. The method for manufacturing a semiconductor memory device of claim 10, wherein in the step (b), the step reducing film is formed by an atmospheric pressure thermal CVD method using O_3 and TEOS.

17. The method for manufacturing a semiconductor memory device of claim 10, wherein in the step (c), the overlying hydrogen barrier film is formed by a sputtering method.

18. A method for manufacturing a semiconductor memory device, comprising the steps of:

(a) forming a first electrode on a semiconductor substrate;

(b) after the step (a), forming an underlying hydrogen barrier film on the substrate;

(c) removing the underlying hydrogen barrier film until a surface of the first electrode is exposed so as to have the first electrode buried in the underlying hydrogen

barrier film;

(d) forming a capacitance insulating film on the first electrode;

(e) forming a second electrode film on the capacitance insulating film;

(f) patterning the capacitance insulating film and the second electrode film so as to form a memory cell capacitor;

(g) after the step (f), forming a step reducing film on the substrate so as to cover the memory cell capacitor; and

(h) forming an overlying hydrogen barrier film on the substrate so as to cover the step reducing film.

19. The method for manufacturing a semiconductor memory device of claim 18, further comprising the step of:

(i) after the step (g), removing the step reducing film in a peripheral region around the memory cell capacitor,

wherein in the step (h), the overlying hydrogen barrier film is formed so as to be in contact with the underlying hydrogen barrier film in the peripheral region around the memory cell capacitor.

20. The method for manufacturing a semiconductor memory device of claim 18, wherein in the step (g), the step reducing film is formed by an atmospheric pressure thermal CVD method using O_3 and TEOS.

21. The method for manufacturing a semiconductor

memory device of claim 18, wherein in the step (h), the overlying hydrogen barrier film is formed by a sputtering method.